WHAT IS CLAIMED IS:

1. A method for correcting crosstalk in layout designing of a semiconductor integrated circuit, comprising:

the step of a first checking of a parallel wiring length, wherein data of a parallel wiring length allowable value and layout data regarding crosstalk are input to extract information of parallel wiring length infringement based on both the input data;

the step of searching for an empty space, wherein cell area information is input and the empty space is searched for on an infringing wiring route included in the information of parallel wiring length infringement while referring to the cell area information to extract empty space information;

the step of creating a candidate for buffer division, wherein a plurality of inverters to be divided from a driving buffer of the infringing wiring part or a driving buffer at the next stage are extracted as a candidate for crosstalk correction;

the step of arranging and wiring, wherein the inverters as the candidate for crosstalk correction are arranged and wired in the empty space included in the empty space information; and

the step of a second checking of the parallel wiring length, wherein parallel wiring length infringement is checked with respect to the inverters newly arranged.

2. A method for correcting crosstalk in layout designing of a semiconductor integrated circuit, comprising:

the step of the first checking of a parallel wiring length, wherein data of a parallel wiring length allowable value and layout data regarding crosstalk are input to

extract information of parallel wiring length infringement based on both the input data;

the step of searching for an empty space, wherein cell area information is input and the empty space is searched for on an infringing wiring route included in the information of parallel wiring length infringement while referring to the cell area information to extract empty space information;

the step of creating a candidate for cell movement, wherein a cell to be moved out of a driving cell of the infringing wiring part and a driving cell at the next stage is extracted as a candidate for crosstalk correction;

the step of arranging and wiring, wherein the cell as the candidate for crosstalk correction is arranged and wired in the empty space included in the empty space information; and

the step of a second checking of the parallel wiring length, wherein parallel wiring length infringement is checked with respect to the cell newly arranged.

3. A method for correcting crosstalk in layout designing of a semiconductor integrated circuit, comprising:

the step of a first checking of a parallel wiring length, wherein data of a parallel wiring length allowable value and layout data regarding crosstalk are input to extract information of parallel wiring length infringement based on both the input data;

the step of searching for an empty space, wherein cell area information is input and the empty space is searched for on an infringing wiring route included in the information of parallel wiring length infringement while referring to the cell area information to extract empty space information;

the step of victim net logic synthesis, wherein logic connection information is input and a candidate for crosstalk correction is extracted, in which logic of a net part including the parallel wiring length infringing wiring is resynthesized based on the logic connection information to increase the number of elements to be arranged or to change fan-outs for correcting the crosstalk infringement;

the step of arranging and wiring, wherein based on the candidate for crosstalk correction, a cell is arranged and wired in the empty space included in the empty space information; and

the step of a second checking of the parallel wiring length, wherein parallel wiring length infringement is checked with respect to the new corrected circuit.

4. A method for correcting crosstalk in layout designing of a semiconductor integrated circuit, comprising:

the step of crosstalk analysis, wherein logic connection information, RC information, analytical limitation information, delay library, and crosstalk analysis library are input to perform delay calculation and timing analysis in view of delay variation due to crosstalk caused by synchronous transitions from a timing window based on the input information and the like, and crosstalk infringement information which includes wiring with crosstalk generated and timing window data are extracted;

the step of searching for an empty space, wherein cell area information is input and the empty space is searched for on a wiring route adjacent to the position with the crosstalk generated which is included in the crosstalk infringement information while referring to the cell area information to extract empty space information;

the step of logic synthesis of both aggressor and

victim nets, wherein a candidate for crosstalk correction is extracted, in which the empty space information and the timing window data are referred to, logic of an affecting side and an affected side of the wiring nets with crosstalk generated is decomposed, synchronous in-phase transition is inverted to opposite-phase transition or opposite-phase transition to in-phase transition, and the delay variation is changed so as to keep the safe side with respect to timing limitation;

the step of arranging and wiring, wherein the cell is arranged and wired based on the candidate for crosstalk correction; and

the step of a second crosstalk analysis, wherein the crosstalk infringement is checked with respect to the new corrected circuit.

5. A method for correcting crosstalk in layout designing of a semiconductor integrated circuit, comprising:

the step of crosstalk analysis, wherein logic connection information, RC information, analytical limitation information, delay library, and crosstalk analysis library are input to perform delay calculation and timing analysis in view of delay variation due to crosstalk caused by synchronous transitions from a timing window based on the input information and the like, and slack data which includes timing limitation infringement information and timing window data are extracted;

the step of extracting a net to be corrected, wherein the net to be corrected which has coupling capacitance exceeding a predetermined value with adjacent wiring is extracted from nets on timing limitation infringing paths which are included in the slack data,

the step of searching for an empty space, wherein

cell area information is input and referring to the cell area information, the empty space is searched for on a wiring route having the coupling capacitance which is included in the information of the net to be corrected to extract empty space information;

the step of logic synthesis of the timing limitation infringing path, wherein a candidate for crosstalk correction is extracted, in which the empty space information and the timing window data are referred to, the logic synthesis in which logic of the nets including the adjacent wiring parts is decomposed or the number of fan-outs thereof is changed is performed to find signal transitions between the adjacent wiring to be synchronous, and in the case of hold infringement, to inverse the transition to be in-phase while in the case of setup infringement, to be opposite-phase;

the step of arranging and wiring, wherein a cell is arranged and wired based on the candidate for crosstalk correction; and

the step of the second crosstalk analysis, wherein the crosstalk infringement is checked with respect to the new corrected circuit.